

# Resist Profile Aware Source Mask Optimization

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## ABSTRACT

In this paper, we present the approach and results of resist profile aware source mask optimization (SMO). In this approach, the cost functions for optimization include the image properties calculated not only from the resist bottom image planes, but also from the top image planes. Consequently, the optimized source and mask shapes are a good balance between the process window for the bottom CD's, and top CD control to ensure a straight resist profile favorable for the etching process. We built up the flow of resist profile aware SMO and implemented it on a 1x nm node back-end layer. Two best candidate sources, SMO1 and SMO2 were generated from the conventional SMO flow and the resist profile aware SMO flow, respectively. The simulation results indicate that a better resist profile is achieved by SMO2, although it gives rise to a relatively smaller overlapping process window evaluated at the resist bottom. Wafer data including bottom CD measurement for critical pattern clips and cross-sectional SEM images from selected patterns have shown good matching with the simulation results, indicating that resist-profile aware SMO is a feasible approach to optimize the illumination sources for a reasonable bottom CD based process window as well as favorable resist profiles.

**Keywords:** SMO, resist profile, process window, overlapping depth of focus, OPC model, edge placement error

## 1. INTRODUCTION

The control of resist profile has become very important in advanced lithography, as it plays a critical role in determining the post-etch final CD's. Although the resist profile is co-related to the resist chemistry and is normally tuned under certain baking/developing conditions, it can also be optimized by engineering the optical intensity distribution through the resist thickness. One such method is the resist profile aware Optical Proximity Correction (OPC), in which the resist top CD's are calculated and their edge placement errors (EPE's) are added into the cost function of OPC. As a result, the final mask layout shapes are tailored for a better top CD control, while the bottom CD contour accuracy is reasonably maintained [1]. In addition to the mask layout shapes, the illumination source also has a significant effect on the image intensity distribution and thus opens another way for resist profile engineering.

Source Mask Optimization (SMO) [2-6] has become one of the key resolution enhanced techniques in lithography and has been widely used for 2x nm nodes and below. SMO is meant to seek the optimized source/mask combinations based on certain cost functions constructed from the image properties over a given set of critical pattern clips. The image properties defined in the cost function can be purely optical properties such as the image slope near the target edge, or EPE's calculated with an OPC model [5] or with a rigorous lithography model [6]. In any case, the image properties are computed from an aerial image plane near the resist bottom. Hence, the optimized source is supposed to give the maximum process window evaluated at that particular image plane. It is totally unknown how the optimized source would affect the resist profile.

In the resist profile aware SMO approach described in this paper, we introduce another aerial image plane near the resist top and add the image properties from that plane into the metric for optimization as well. As a result, the optimized source will exhibit advantages not only in the bottom CD based process window, but also in the control of top CD and resist profile. To prove this concept, we implemented the resist profile aware SMO on a 1x nm back-end layer that requires critical control of resist profile. The performance of the source generated from resist profile aware SMO was compared with that from conventional SMO by both simulation and wafer results.

The paper is organized as follows. The methodology and flow of resist profile aware SMO is described in Section 2. The results and discussion from the case study are then given in Section 3, with the simulation data and wafer data presented in two sub-sections. Finally, the conclusion is drawn in Section 4.

## 2. METHODOLOGY

### 2.1 Methodology of resist profile aware SMO

In the typical Tachyon SMO approach, the cost function is defined as the sum of EPE's of the critical pattern clips at multiple process conditions and certain penalty terms that account for SRAF printing, side-lobe printing, etc. Aiming at the maximization of the process windows, i.e. smaller CD variations with respect to dose, defocus and mask size variations, the process conditions at which the EPE's are calculated normally include the nominal condition, defocus conditions, off-dose conditions, and conditions with mask errors. As a result, the optimized source-mask combination is supposed to give rise to the best depth of focus (DOF), exposure latitude (EL) and mask error enhancement factor (MEEF) for that pool of critical pattern clips. In our method, calibrated OPC models for a reference source are normally used to calculate the EPE's, which is believed to give superior results over a purely optical model with a constant threshold. The OPC model is generally calibrated at a certain aerial image plane near the resist bottom, which correlates to the resist z-plane where the bottom CD is extracted from the CDSEM measurement. Hence, it is the contour EPE's from that aerial image plane that are minimized in SMO. Thus, the process windows are optimized for the bottom CD's that can be readily characterized by CDSEM measurement. In this whole process, all the characterization, calculation, and optimization are actually carried out for one bottom image plane.

To take the resist profile into consideration for SMO, the EPE's from another aerial image plane near the resist top can be added into the cost function for optimization, making it a resist profile aware SMO. If a source is optimized at the two image planes and yields small EPE's for the same target on both planes, it is supposed to give a straight resist profile and probably small top loss favorable for the etching process. To calculate the EPE's from the top image plane, another OPC model is required. For the positive-tone developing (PTD) process, a good approximate model can be generated simply by moving the aerial image location of the OPC model to the corresponding top image plane. In this case, there are no extra requirements to start resist profile aware SMO. If a resist profile model such as the Tachyon R3D model [7] is available, it can be used to extract EPE's from any aerial image plane and is a natural choice for resist profile aware SMO. A resist profile model is a pre-requisite to start resist profile aware SMO for the negative-tone developing (NTD) process, because the aerial image plane extrapolation method does not give a correct across-thickness CD trend for the NTD process.

### 2.2 Flow of resist profile aware SMO

The flow of resist profile aware SMO is illustrated in Figure 1. First, a sub-set of critical pattern clips are selected by using the diffraction based approach [5]. If there are known weak points related to the resist profile, they should be included as well. The cost function for optimization is then defined by identifying the aerial image planes and relevant process conditions from which the EPE's of the critical patterns are calculated. While the bottom image plane follows what is defined in the OPC model, there are no obvious rules on how to select the top image plane. Nevertheless, a good starting point should not be too close to the resist top, where the EPE's get very large and tend to dominate the whole optimization process, resulting in a poor process window at the resist bottom.

With the cost function in place, the SMO is run by using the well-established algorithm. The results of SMO should be examined by looking at both the process window evaluated at the bottom image plane and the EPE's at the top image plane. Since these two metrics are always competing with each other, a good balance point may only be reached after a few cycles. Once the candidate source gives sufficient bottom-CD based process window as well as satisfactory top image EPE's, we can proceed with source verification over the whole critical pattern clip pool.

As shown in Figure 1, the candidate source is verified by calculating its best process window achievable by mask optimization (MO). The cost function definition in MO can exactly follow that from SMO. One interesting point here is that the mask shapes do have impact on the resist profile. Hence, if one would like to investigate the pure source effect on the resist profile, the cost function for MO can be defined in such a way that EPE's from only the bottom image plane are included.

Finally, if the source verification results on all the critical patterns are comparable with what has been achieved on selected critical patterns by SMO, the candidate source is considered to be qualified by simulation and can be installed

on scanners for wafer verification. For full-chip applications, OPC recipe tuning and weak point verification for the optimized source are required, in which the top image contours may also be taken into consideration during correction. The practice for the relevant full-chip weak point verification is not discussed in this paper.

In summary, the whole resist profile aware SMO flow is built upon the current SMO framework, with the only difference in the optimization metric definition. Hence, the implementation of resist profile aware SMO on real cases is straightforward.

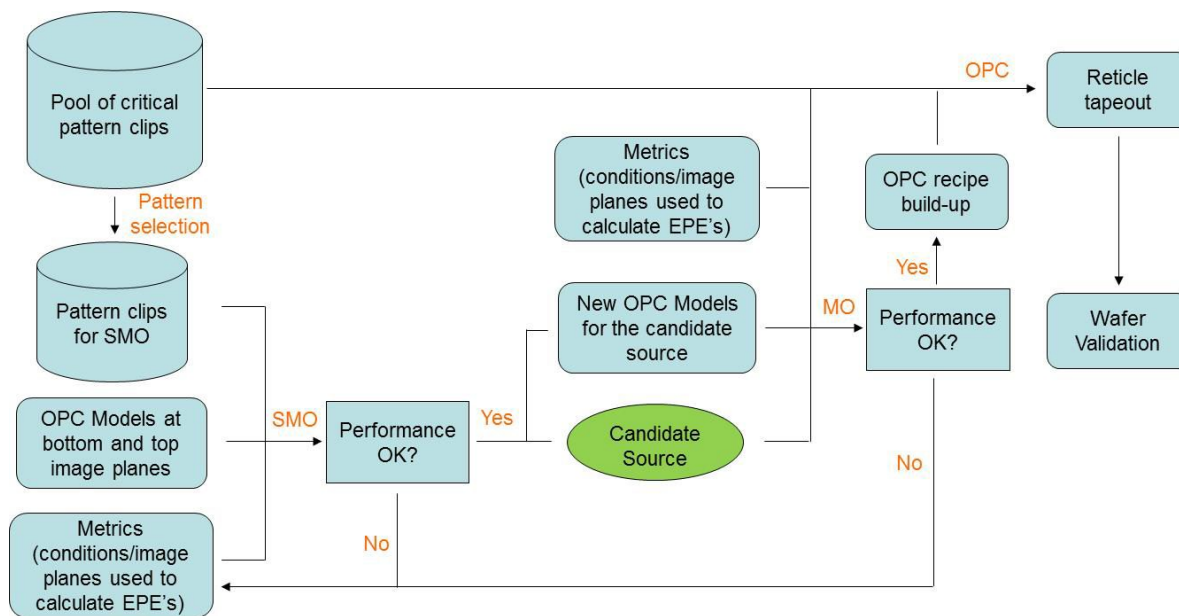


Figure 1. Flow of resist profile aware SMO

### 3. RESULTS AND DISCUSSION

#### 3.1 Simulation data

The resist profile aware SMO methodology described in the previous section was implemented on a 1x nm node back-end layer. The PTD resist process is used for this layer, for which one OPC model calibrated for a reference source is available prior to the study. The aerial image plane defined in the OPC model is located at about 2/3 of the resist thickness starting from the top. To enable the computation of the EPE's at the top image plane, we generated an OPC model by moving the aerial image location of the existing OPC model to about 1/3 of the resist thickness starting from the top.

Around 80 critical pattern clips were then identified for this layer, about half of which were selected to generate candidate sources through the conventional SMO flow as well as the resist profile aware SMO flow. Figure 2 illustrates the process conditions at which EPE's were calculated and incorporated into the metric for SMO. In the conventional SMO flow, 7 conditions including the nominal condition from the bottom image plane were considered, covering process variations in dose, defocus, and mask errors. In addition to these 7 conditions, the nominal EPE's from the top image plane were also included with an equal weight for the resist profile aware SMO. Such a combination has proven to be a good balance between the maximization of bottom CD based process window and top image EPE's for this test case. Two best candidate sources, SMO1 and SMO2, were obtained from the conventional SMO and resist profile aware SMO, respectively.

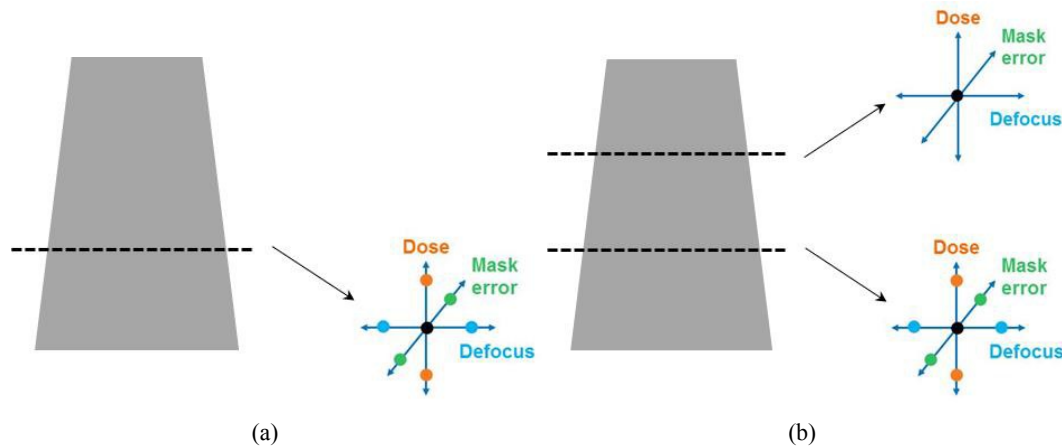


Figure 2. Process conditions at which EPE's were calculated and incorporated into the metric for (a) conventional SMO; (b) resist profile aware SMO

Following the flow described in Section 2.2, the performance of the two candidate sources was verified over all the critical pattern clips. To visualize the benefit for resist profile that is solely contributed by the source, only the EPE's from the bottom image plane were incorporated into the cost function for MO. The results of bottom CD based process window are summarized in Figure 3 and Figure 4. As shown in Figure 3, significant improvement of the overlapping process window over the reference source was achieved by both sources. More quantitative results are given by the EL vs. DOF plots in Figure 4. Based on 10% bottom CD variation, the overlapping DOF at 5% EL is 86 nm for the reference source, which is improved to 124 nm and 106 nm by SMO1 and SMO2, respectively. It is expected that the best bottom CD based DOF improvement is achieved by using SMO1, as its cost function is meant for the optimization of the bottom image EPE's only. Nevertheless, the DOF given by SMO2 is good enough to meet the lithography process requirements.

To evaluate the resist profile given by the two candidate sources, the EPE's of the critical patterns from the top image plane were compared. As shown in Figure 5(a), the top image EPE's given by SMO2 are smaller for all the critical patterns, which is a direct verification of the impact given by the intentional cost function adjustment. Only representative critical patterns are shown in the plot for better visualization, which cover all pattern types, pitches and target CD range. Since the simulated contours are available from two image planes, the top CD-to-bottom CD difference at the nominal condition is then plotted in Figure 5(b). It is observed that a smaller top CD-to-bottom CD difference is achieved by SMO2 for almost all the critical pattern clips, indicating that less tapered resist profiles are given by SMO2. Finally, the overlapping process windows of all the critical patterns from both the bottom and the top image planes are plotted on the same graph, as shown in Figure 6. For SMO1, although the individual overlapping process windows are large for both the bottom and top image planes, there is no overlap between them. On the other hand, SMO2 gives good common overlapping windows. Considering that only the bottom image EPE's are included in the metric for source verification, the advantages for resist profile shown here are ascribed to the source only.

While the concept of resist profile aware SMO is successfully demonstrated by simulation, further investigation is required to establish more details about the best practice. First, there is a large flexibility regarding how the cost functions should be constructed. A more systematic way to determine the location of the top image plane and its associated process conditions for EPE computation is needed. Second, in addition to the top image EPE's, other quantitative gauges to evaluate the resist profile are required. One possible criterion could be the pinching/bridging specifications defined for the top image planes, which can be linked to the requirements for the etching process.

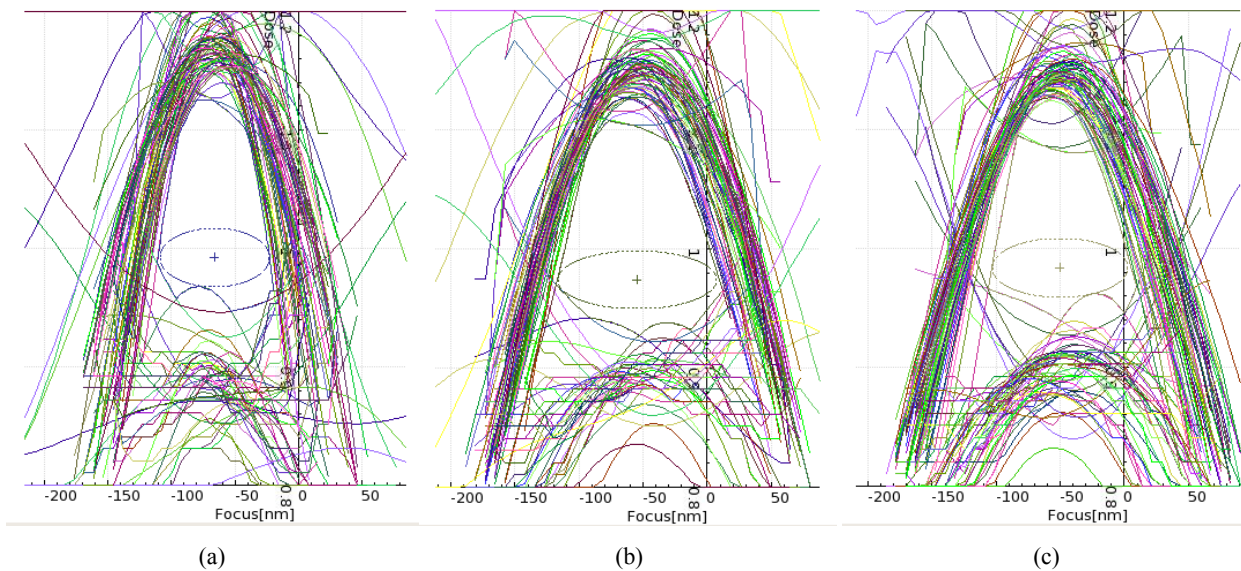


Figure 3. Process window plots of all the critical patterns simulated for the verification of (a) reference source; (b) SMO1 (R2D); (c) SMO2 (R3D) through mask optimization.

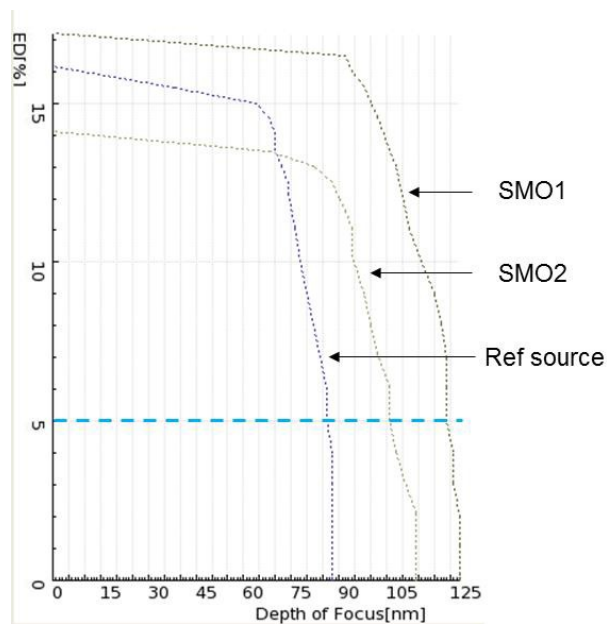
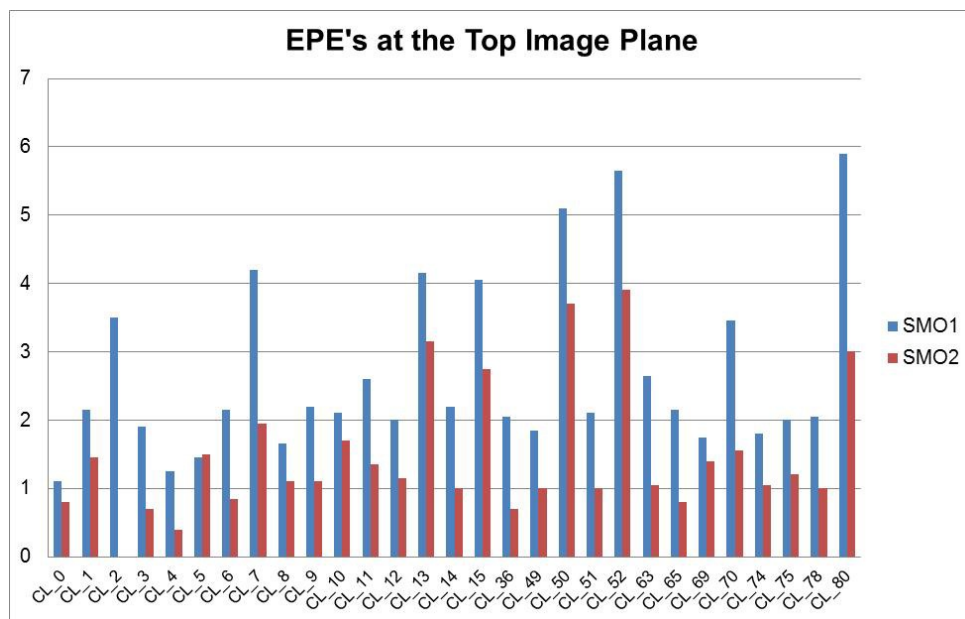
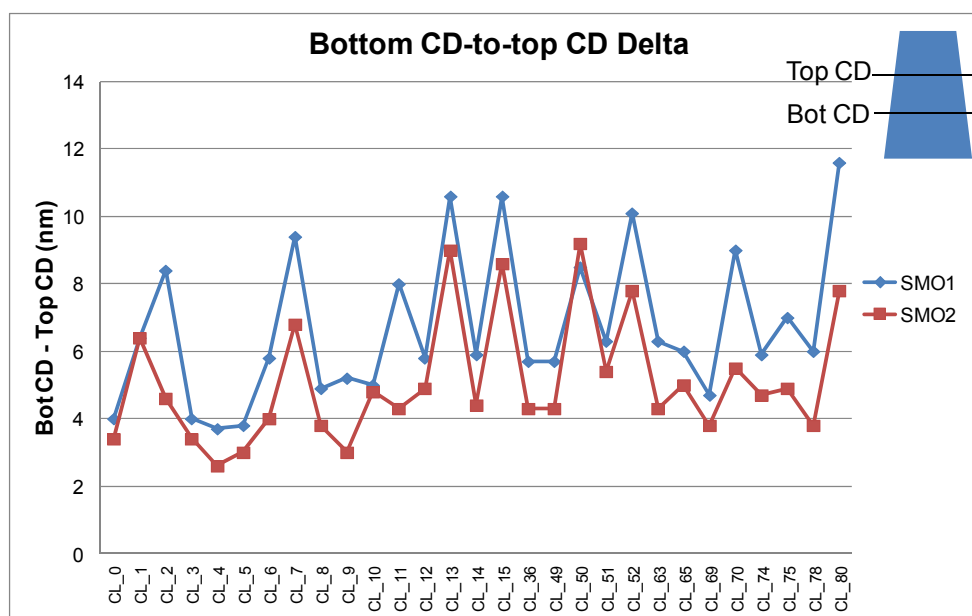


Figure 4. Exposure latitude vs. depth of focus calculated based on 10% bottom CD variation for the reference source, SMO1 (R2D), and SMO2 (R3D).



(a)



(b)

Figure 5. (a) Comparison of top image EPE's from SMO1 (R2D) and SMO2 (R3D). A smaller EPE is achieved by SMO2 for every critical pattern clip; (b) simulated resist bottom CD-to-top CD delta for critical patterns from the two candidate sources.



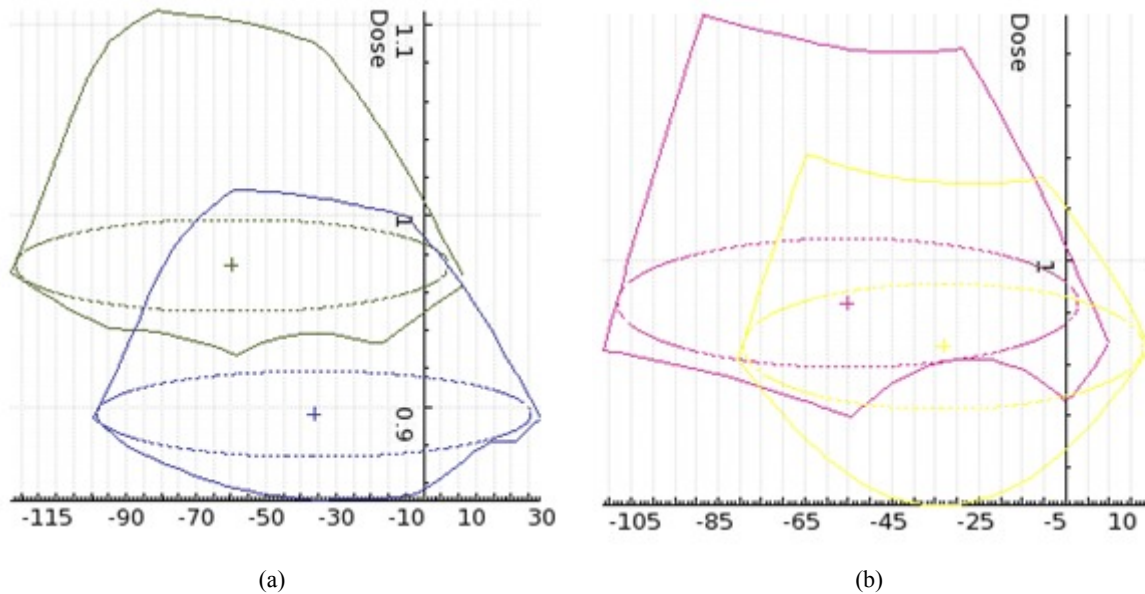


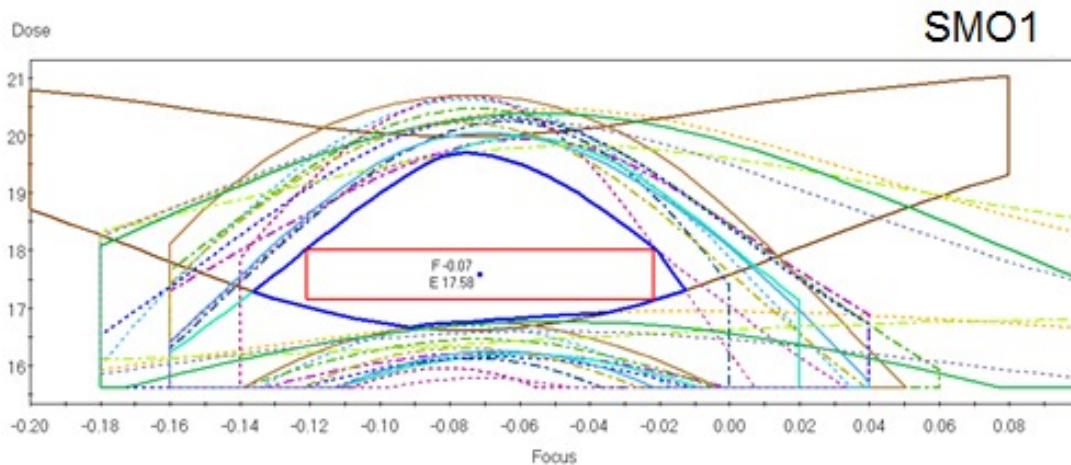
Figure 6. Overlapping process windows for all the critical patterns from both the bottom and top image planes for (a) SMO1 (R2D); (b) SMO2 (R3D)

### 3.2 Wafer data

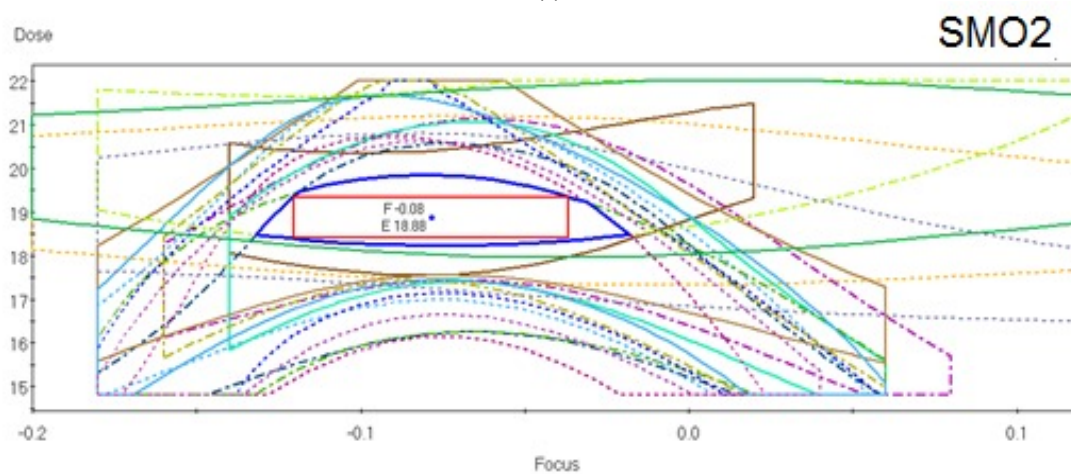
To verify the performance of the candidate sources on real Si, two sets of OPC recipes were built up for SMO1 and SMO2, respectively. Resist top CD's were not included into the cost function of OPC. Test chips and test pattern macros including the critical pattern clips used for SMO were run through the two OPC splits and were placed on the same test mask for wafer verification.

Two wafers were exposed with a focus-exposure matrix (FEM) by using SMO1 and SMO2, respectively. Full-map CD's were then measured for over 30 representative critical patterns from the two FEM wafers. The process window plots for the two wafers are shown in Figure 7. Decent process windows were achieved by both sources. Based on 10% bottom CD variation, the overlapping DOF at 5% EL is 99 nm and 84 nm for SMO1 and SMO2, respectively. It is worth pointing out that the rectangular DOF's are calculated from the wafer data, which are generally smaller than the elliptical DOF's shown in Figure 3 for the simulation data. If we re-calculate the corresponding rectangular DOF from the simulation results, the overlapping DOF for SMO1 and SMO2 are 106 nm and 94 nm, respectively, which shows a close matching with the wafer results.

The characterization of the resist profile is much more challenging than the bottom CD measurement. Typical approaches include cross-sectional SEM and AFM, but both are limited to a low throughput. The cross-sectional SEM images of dense and isolated resist lines from two focus-stripe wafers exposed with SMO1 and SMO2 are given in Figure 8. The two wafers were processed on the track at the same time to minimize any possible effect on the resist profile caused by resist process variations. As shown in Figure 8, while the resist profiles from SMO1 shows evident top rounding, the profiles from SMO2 exhibit much straighter sidewalls for both dense and isolated line structures. These results illustrate the strong effect of the illumination source over the resist profile, and are a good proof of the advantages given by resist profile aware SMO. The characterization by cross-sectional SEM, however, is limited to simple 1D patterns. For 2D structures that have generally more tapered resist profiles and are more sensitive to top loss, other characterization methods are required. Our next plan is to investigate the weak points resulting from the resist top image plane, which can be well captured by CDSEM measurements.

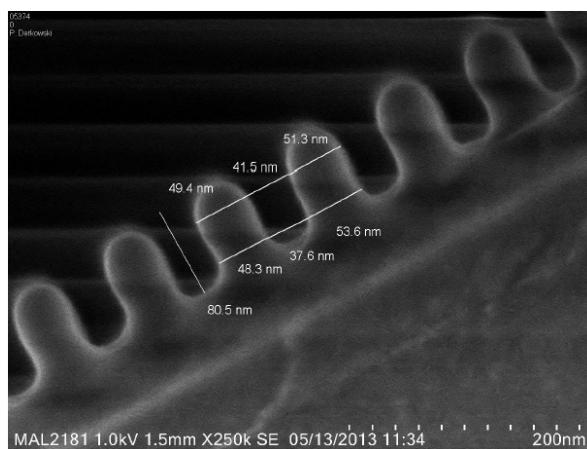


(a)

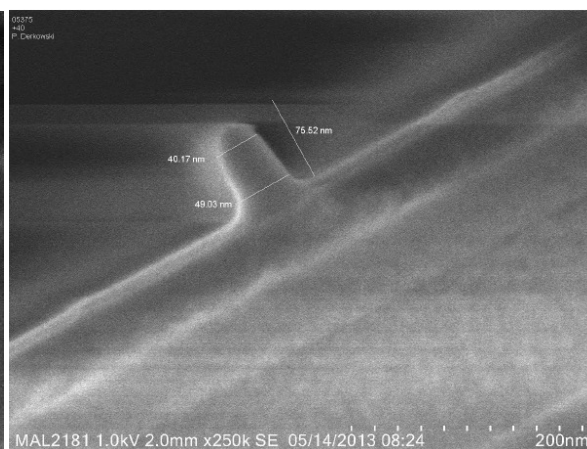


(b)

Figure 7. Process window plots constructed by using the full-map bottom CD data measured from two FEM wafers exposed by using the source of (a) SMO1 (R2D); (b) SMO2 (R3D).



(a)



(b)



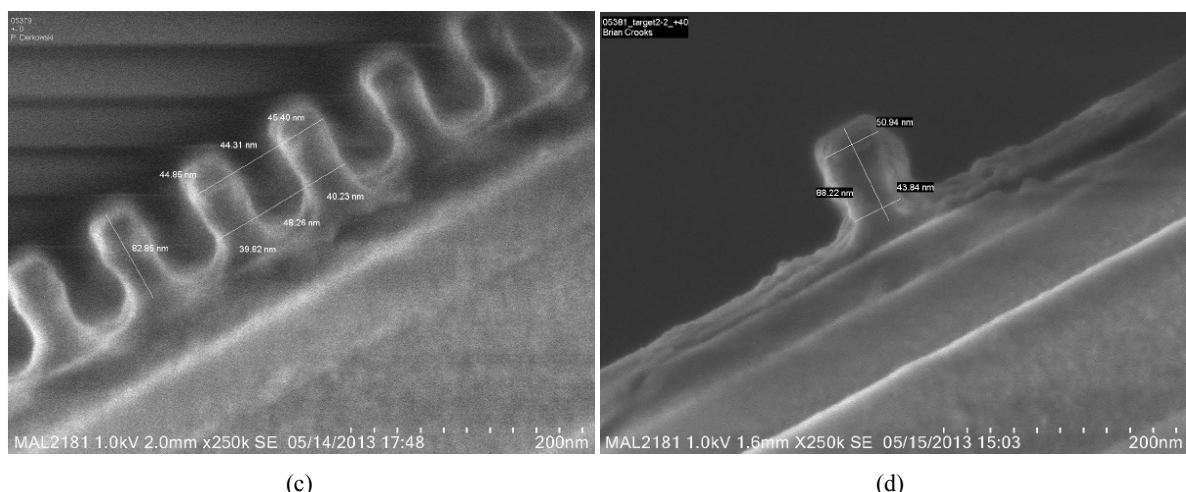


Figure 8. Cross-sectional SEM images for dense and isolated line structures. (a) and (b) are from the focus-stripe wafer exposed with the source of SMO1 (R2D). (c) and (d) are from the focus-stripe wafer exposed with the source of SMO2 (R3D). The dense lines (a) and (c) are from a nominal defocus field, while the isolated lines (b) and (d) are from a field with +40 nm focus shift from the nominal defocus.

## 4. CONCLUSION

We have demonstrated the approach of resist profile aware SMO, in which the EPE's of critical pattern clips from both the top and bottom image planes are included into the metric for optimization. One case study has been carried out by implementing both resist profile aware SMO and conventional SMO over the same set of critical pattern clips. As indicated by both simulation and wafer results, although the source generated by resist profile aware SMO gives rise to a relatively smaller overlapping DOF evaluated at bottom CD, it shows clear advantages in resist profiles for the critical patterns. Furthermore, the bottom CD based process windows given by resist profile aware SMO are good enough to meet the process requirements. Therefore, we believe the resist-profile aware SMO is a feasible approach to optimize the illumination source for a reasonable bottom CD based process window as well as favorable resist profiles. More work is in progress to make the flow of resist profile aware SMO more systematic and implement it for full-chip applications.

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